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(54) Multiprocessor cache system.

(57) The bandwidth of the data transfer among a main memory and snoopy caches is improved by solving the bus neck in a multiprocessor system using a snoopy cache technique. Shared bus coupling is employed for an address/ command bus 5 requiring bus snoop whereas multiple data paths coupled by an interconnection network 7 are used for the data bus not requiring bus snoop. The multiple data paths 7 reflect the order of the snoopy operations on the order of data transfer such as to maintain data consistency among the caches.

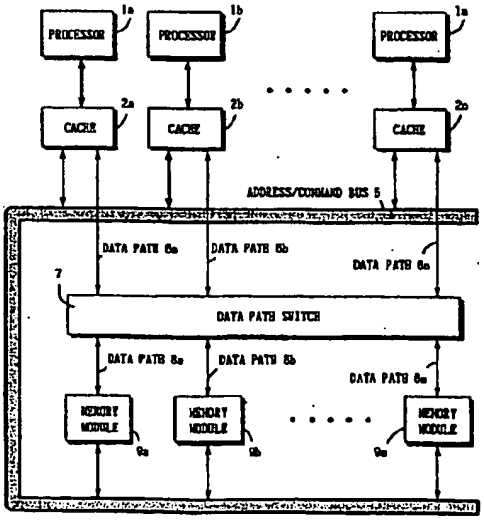

FIG. 2

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